Compatibility Issues Between S3 Savage4 and VIA North Bridge Chips

Introduction

Several problems have been found in certain circumstances when using an S3® Savage4™-based add-in card in a system using a VIA® North Bridge chip. These include typically either an hourglass cursor hang when booting into Windows® or a hang when running an application such as 3DWinBench™ or 3DMark™. Random screen corruption has also been noticed in some instances. This technical note discusses and provides solutions to each of several separate issues related to optimizing the AGP interface of Savage4 designs in VIA systems. The areas discussed are affected products, Savage4 issues, VIA issues and AGP specification issues. A summary provides the problem fix requirements for various VIA North Bridge chips.

Affected Products

All Savage4-based Diamond AGP add-in cards:

- Speedstar A90
- Speedstar A200
- Stealth III S540 (16 and 32 MB)
- Stealth III S540 Xtreme

All Savage4-based AGP products used with a VIA North Bridge.

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Savage4 Issues

Exhaustive failure analysis has determined two areas of Savage4 sensitivity.

1) AGP VREF Noise

   Savage4 is sensitive to noise on the AGP VREF signal. Such noise can translate into an AGP data bus setup time violation for both the 2X and 4X incoming data stream. Since it is an incoming stream, this violation can happen in either AGP pipe or sideband mode. The S3 design alert DA064B (refer to Addendum A) explains in detail how to fix this problem. Resistor changes to the AGP VREF resistor divider circuit are required. S3 has modified its Savage4 chip test program to test production devices at the new AGP VREF settings, thereby ensuring proper operation in systems. This change should be made on all Savage4-based add-in cards.

2) AGP Clock to Strobe Timing

   Savage4 is sensitive to the AGP timing t_{RSh} (AGP Receive Strobe Hold Time from AGP Clock). The Savage4 controller needs a minimum t_{RSh} of 2 ns as opposed to the 1 ns specified by the AGP 2.0 specification. This problem has been noticed ONLY on a VIA VT82C693A motherboard implementation. Measurements on many motherboards (using other North Bridge chips from VIA or chips from ALI, SiS®, Intel® and AMD®) show that these systems provide plenty of margin for the Savage4 requirement.

   Having the AGP clock Spread Spectrum function enabled increases the probability of seeing a failure. Spread Spectrum modifies the AGP clock by modulating its frequency in order to reduce Electro-Magnetic Interference (EMI). Unfortunately, this affects timing and reduces timing margin on the bus, which aggravates the Savage4 t_{RSh} timing sensitivity. Many systems will not allow turning off the Spread Spectrum function because they need this function enabled to meet EMI requirements. The S3 BIOS revision 2.XD.19 implements a solution to the timing problem that works with the Spread Spectrum function enabled. This ensures AGP1X and AGP2X operation on ALL North Bridge devices, including the VIA family.

VIA North Bridge Issues

Here is a table showing the latest VIA North Bridge devices:

Part Number	Product Name	AGP Capability	CPU Bus	Memory Bus	Processor type
VT82C598/598AT	Apollo MVP3	1X, 2X	100 MHz max.	100 MHz max.	Socket-7
VT82C693	Apollo Pro-Plus	1X, 2X	100 MHz max.	100 MHz max.	Slot-1, Socket370
VT82C693A	Apollo Pro133	1X, 2X	133 MHz max.	133 MHz max.	Slot-1, Socket370
VT82C694	Apollo Pro133A	1X, 2X, 4X	133 MHz max.	133 MHz max.	Slot-1, Socket370

The only issue is with the VIA VT82C694 North Bridge chip. This chip has an insufficient VDDq transient current capability, which translates into poor AGP signal quality when the AGP bus is heavily switching. Simultaneous switching outputs require a higher transient current and the higher the frequency the higher the current requirement. This explains why failures appear with AGP4X and not with AGP1X or AGP2X.

The quality of the TRDY# signal is poor. Both overshoot and undershoot on this signal can cause problems. VIA has issued details of a motherboard fix that should be implemented in all systems (refer to Addendum B). The fix involves the insertion of a ferrite bead/capacitor circuit to reduce the noise spikes on the TRDY# signal. Even though no failures have been seen in AGP2X mode, implementation of this change for AGP2X is strongly recommended.

Strobe signals are also severely affected. The AD_STB and AD_STB# signals are not properly driven by revision "CD-E" of the VIA VT82C694 North Bridge chip. AGP4X will not work reliably on motherboards using this revision and therefore systems with this revision should be updated to revision "CD-G" or later. The VIA VT82C694 North Bridge chip revision can be determined by examining the markings on the VIA chip. The revision number is made up of three characters "XY-Z" where "XY" are the fifth and sixth characters of the 2nd line beneath the VIA logo and "Z" is the 3rd character of the 3rd line beneath the VIA logo. The marking appears thus:

VIA LOGO
VT82C694
9940CD TAIWAN
12G ONO800 c m

The example above shows a Revision "CD-G". Note that "CE-B" is a later revision than "CD-G", the second character having precedence over the third one.

AGP Specification Issue

The AGP 2.0 specification does not define which device (North Bridge chip or graphics controller) must disable its 4X capability when the AGP bus is running at 3.3V. Because neither the S3 Savage4 nor the VIA VT92C694 North Bridge chip implements this functionality, an add-in card may boot to Windows in AGP4X with the bus running at 3.3V. This mode is not supported and must be avoided. The S3 Win9X driver revision 8.20.06 fixes this problem.

Summary

Following is a complete list of all problem fixes discussed above:

- AGP VREF (VREFB) fix on Savage4 cards (Fix A; supplied by S3)
- S3 BIOS 2.XD.19 or later used (Fix B; supplied by S3)
- S3 Win9X driver 8.20.06 or later used (Fix C; supplied by S3)
- TRDY# fix is implemented on motherboard (Fix D; supplied by VIA)
- VT82C694 revision "CD-G" or later used (Fix E; supplied by VIA)

The fixes required for reliable operation are shown in the following table:

VIA North Bridge Chip	AGP Type	Fixes Required
VT82C598/598AT, VT82C693, VT82C693A	1X, 2X	A, B
VT82C694	1X, 2X	A, B, C, D
VT82C694	4X	A, B, C, D, E

The Multimedia Division will implement all the S3 fixes on affected products by 4/1/2000. For new business opportunities prior to this date involving a Savage4-based Diamond AGP add-in card and a VIA North Bridge, please call Greg Farris (Product Line Manager) at 1-408-588-8613 to discuss specific supply requirements customers may have before 4/1/2000.

Addendum A

VREFB Noise Sensitivity on Savage4-based Designs (Version B)

Introduction

The S3® Savage4™ reference schematics (Rev. 2.2) include a resistor divider network to generate an AGP reference voltage (VREFB) input to Savage4 when the I/O operating voltage (VDDq) is 3.3V, or use the AGP VREFCG when VDDq is 1.5V (see Figure 1). It has been observed that on certain types of motherboards, the choice of resistor values in the divider network is very critical. Improper selection of resistor values may cause pixel corruption and even system hangs if extreme care is not taken to minimize noise on the VREFB signal.

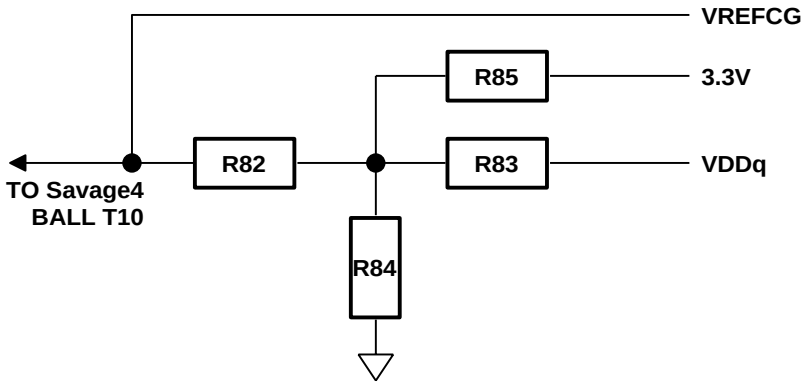

Figure 1

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Failure Modes

The predominant mode of failure is screen background color corruption when dragging windows on the desktop. In addition, specific tests that switch a large number of data bits during every data phase (on the AGP bus) have been shown to fail because of this issue. A Windows® hang is also possible, exhibiting an hourglass cursor or a blue screen.

Analysis and Recommendations

Tests have shown that the failures are the result of the VREFB levels being too low. A Lower VREFB DC level, coupled with AC noise, brings VREFB too low, resulting in loss of margin for the input voltage parameters. Therefore, Savage4 designs MUST raise the VREFB levels in both 1.5V VDDq and 3.3V VDDq environments from that originally recommended. For 1.5V VDDq environments, VREFB should be approximately 0.86V (instead of 0.75V). For 3.3V VDDq environments, VREFB should be approximately 1.54V (instead of 1.32V). Fortunately, this also gives the Savage4 input buffers more setup margin, especially for 4x AGP operation.

Suggested Modifications and Layout Considerations

For designs that may already be in production, S3 recommends that the values for the resistors R82 through R85 be those listed in Table 1. These resistors values were carefully calculated and tested on a large sample including many different Savage4 baseboards as well as many different chipset/motherboard combinations. The resulting VREFB will make the board work robustly in both 3.3V and 1.5V VDDq environments.

Table 1. VREFB Divider Network R Values

Resistor	Ohms (1%)
R82	0
R83	100
R84	69.8
R85	392

S3 strongly recommends that a thorough board qualification test be performed using a manufacturing diagnostic, such as S3 Sleuth, in order to guarantee correct functional operation across a variety of motherboards. In particular, we recommend running tests which enable AGP 2x or 4x functionality and obtaining scope waveforms of the VREFB pin in 'Infinite Persistence' mode. The maximum peak-to-peak deviation on the VREFB pin should approach a maximum of 200 mV.

For new Savage4 AGP designs, S3 recommends that particular attention be paid to the layout of the VREFB trace. As stated in the AGP 2.0 specification, section 4.3.5, the VREFB divider network should be as close to the receiver as possible. In addition, section 4.3.6 of the AGP 2.0 specification (found on the web at http://www.intel.com/technology/agp/agp_index.htm) states that the VREFB divider network for AGP 4x operation, should be placed as close to the AGP interface as is practical to get the benefit of the common mode power supply effects. The trace spacing around the VREFB signal must be a **minimum** of 25mils or 5x the dielectric thickness, whichever is greater, to reduce crosstalk and maintain signal integrity. Typical dielectric thicknesses used in the PCB manufacturing process range between 4.0mils and 4.5mils. For new Savage4 AGP designs where layout space is available, a 1.0uF tantalum capacitor may be used in addition to the 0.01uF capacitor on the VREFB trace to further minimize noise.

Addendum B

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Glitch Patch for GFRAME# and GTRDY# of VIA VT82C694X

Date: October 30, 1999

In VIA Apollo Pro133A (VT82C694X) based system, two solutions for the glitch on GFRAME# and GTRDY# are described in this document. The concept of both solutions is to filter the glitch incurred on both GFRAME# and GTRDY# signals between VT82C694X North Bridge controller and the AGP slot. The way to filter the glitch is to add a RC or LC circuit into the signals. Referring to Figure 1, the first solution is to add a 10~15 ohm series resistor and a 5~15 pF ceramic capacitor to ground near the AGP slot. The second solution is to add a 31 ohm (impedance at 100MHz) ferrite bead and a 5~15 pF ceramic capacitor to ground near the AGP slot in Figure 2.

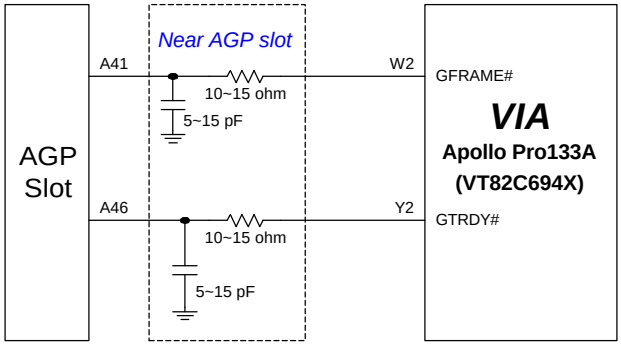

Figure 1. RC circuit for GFRAME# and GTRDY#

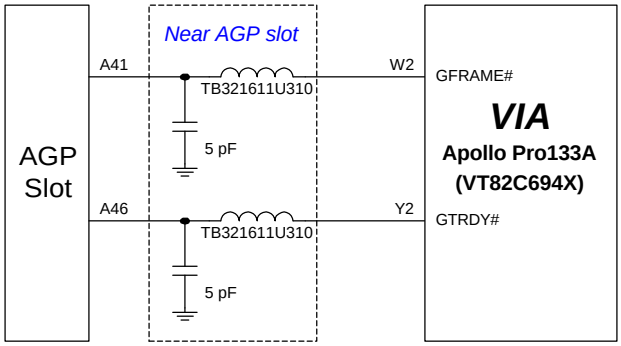

Figure 2. LC circuit for GFRAME# and GTRDY#

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